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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,800	12/10/2001	Jean Louis Calvignac	RAL920000126US1	6069
25299	7590	07/23/2004	EXAMINER	
IBM CORPORATION PO BOX 12195 DEPT 9CCA, BLDG 002 RESEARCH TRIANGLE PARK, NC 27709			AUVE, GLENN ALLEN	
			ART UNIT	PAPER NUMBER
			2111	

DATE MAILED: 07/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/016,800	CALVIGNAC ET AL.
	Examiner	Art Unit
	Glenn A. Auve	2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is **FINAL**.                                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 25 is/are allowed.
- 6) Claim(s) 1-24, 26 and 27 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 10 December 2001 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All
  - b) Some \*
  - c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

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**Attachment(s)**

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/10/2001.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected because it is not clear what is meant by "one of each being located on the first substrate and the second substrate onto the Chip to Chip Bus Interface subsystem" on lines 11-12.

Claims 2-10,23, and 24 are rejected because they depend on claim 1.

Claim 6 is also rejected based on lack of positive antecedent basis of "said second transmission systems" on lines 2-3.

Claim 9 is also rejected because it is not clear what is meant by "a generator response to the one of said requests to generate a message..." on lines 4-5.

Claim 11 is rejected because it is not clear what is meant by "a relatively wide data bus" on lines 9 and 10. It is not clear what constitutes "wide" or "relatively wide".

Claims 12-17 are rejected because they depend on claim 11.

Claim 13 is also rejected based on lack of positive antecedent basis of "the messages having a first footprint" on line 3, "the messages" on line 4, "said messages" on line 5; and "the extracted message" on line 7. Claim 11 also recites "a message" so it is not clear which message or messages are being referred to in claim 13.

Claim 18 is rejected because it is not clear what is meant by "a wide internal ASIC bus" on line 10. It is not clear what constitutes "wide".

Claims 19-22 are rejected because they depend on claim 18.

Claim 13 is also rejected based on lack of positive antecedent basis of "the message" on line 3 because a plurality of messages was previously recited.

***Claim Objections***

3. Claims 5 and 6 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only; in this case they depend on claims 2 and 4 which is not a proper use of multiple dependency. See MPEP § 608.01(n). Accordingly, the claims will not be further treated on the merits.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,2, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Finney et al., U.S. Pat. No. 5,845,072 (Finney).

As per claim 1, Finney shows a system comprising: a first ASIC (Application Specific Integrated Circuit) including a first substrate (Fig. 1,30); a plurality of On Chip Macros mounted on said first substrate (the various elements shown as part of chip 30 and also in fig. 3); a second ASIC including a second substrate positioned in spaced relationship to said first substrate (either 32 or 34); a plurality of On Chip Macros mounted on said second substrate (the elements shown as part of element 32 or 34 in fig. 1 and also in figures 4 or 5); a Chip to Chip Bus Interface subsystem operatively positioned to provide communications between the first

ASIC and the second ASIC (the "CBI" elements and the data bus interfaces in figs. 1 and 3-5); and a Chip to Chip Macro subsystem operatively mounted on the first ASIC and the second ASIC, said Chip to Chip Macro subsystem aggregating all communications between at least a pair of On Chip Macros one of each being located on the first substrate and the second substrate onto the Chip to Chip Bus Interface subsystem (as noted above, the control bus and data bus interface elements in figs. 1 and 3-5). Finney shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Finney also shows that the Chip to Chip bus interface subsystem includes a first transmission system transmitting data from the first ASIC to the second ASIC (fig.3, the control bus master element); and a second transmission system transmitting data from the second ASIC to the first ASIC (in fig.4 or 5, the control bus master elements). Finney shows all of the elements recited in claim 2.

As for claim 7, the argument for claim 1 applies. Finney also shows that the Chip to Chip Macro subsystem includes a first Chip to Chip Macro operatively mounted on the first ASIC; and a second Chip to Chip macro operatively mounted on the second ASIC (throughout the specification wherein the elements 30,32, and 34 are all described as being different chips). Finney shows all of the elements recited in claim 7.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 26 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Luke et al., U.S. Pat. No. 6,505,267 B2 (Luke).

As per claim 26, Luke shows a device comprising: an ASIC having circuits that can be grouped into separate sub Macros (16); and a Chip to Chip Macro mounted on said ASIC, said Chip to Chip macro receiving data at a first data rate with a first footprint from selected ones of said sub Macros converting the data to a second footprint at a second data rate and transmitting the data at the second data rate and second footprint (abstract, fig.2, and cols. 2-3, which describe how serial data is converted by the ASIC 16 to parallel data and vice versa to interface the parallel device to the USB host). Luke shows all of the elements recited in claim 26.

As for claim 27, the argument for claim 26 applies. Luke also shows that the second footprint is narrower than the first footprint and the second data rate is higher than the first data rate (the serial bus has the narrow footprint than the parallel bus and the USB data rate will be higher than the parallel bus transfer rate). Luke shows all of the elements recited in claim 27.

#### ***Allowable Subject Matter***

8. Claim 25 is allowed.

9. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not show the specific chips and macros as recited in claim 25.

#### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references show other macro/ASIC devices or buffering data between different buses.

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11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (703) 305-9638. The examiner can normally be reached on M-Th 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Glenn A. Auve  
Primary Examiner  
Art Unit 2111

gaa  
July 21, 2004

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